REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated December 15, 2006 (U.S. Patent Office Paper No. 12092005). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 11-15 stand for consideration in this application, wherein claims 1-10 are being canceled without prejudice or disclaimer. In addition, new claims 11-15 are hereby submitted for consideration. All amendments to the application are fully supported therein. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Obviousness Double Patenting Rejection

Claims 1-10 were rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U. S. Patent No. 6,911,082. This rejection is respectfully traversed for the reasons set forth below.

As mentioned above, claims 1-10 are being canceled, and now claims 11-15 are being added. Claim 11 is an independent claim, and claims 12-15 depend upon claim 11.

The present invention as now recited in claim 11, however, includes a data select circuit configured to select digital image data received from the first image signal input terminal at a timing of a voltage change from the first voltage to the second voltage as a first digital image data and at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal as a second digital image data and an image signal output circuit configured to output the digital image data received from the first image signal input terminal to the second liquid crystal drive circuit via the second image signal line. These elements are not recited in claim 1 of US Pat. No. 6,862,015. In addition, the present invention as now recited in claim 11 does not include a data storage circuit recited in claim 1

of US Pat. No. 6,862,015. Accordingly, the present invention as recited in claims 11-15 is not obvious over US. Pat. No. 6,862,015.

Prior Art Rejections

35 U.S.C. §103(a) rejection

Claims 1, 2, 4-6, 8-10 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Someya et al. (US Pat. No. 5,091,784) in view of Sasaki et al (US Pat. No. 6,211,849). Also, Claims 3 and 7 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Someya and Sasaki and further in view of Murata et al. (US Pat. No. 6,144,355). As mentioned above, claims 1-10 are being canceled, and new claims 11-15 are being added.

According to the Manual of Patent Examining Procedure (M.P.E.P. §2143),

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both not found in the prior art, not in the applicant's disclosure.

The present invention is directed to a liquid crystal display device capable of performing compensation of any possible variation in duty ratio of clock signals as input to liquid crystal driver circuitry and correct execution of image signal accepting or importing operation to improve display quality. Particularly, the present invention as now recited in claim 11 provides that the first liquid crystal drive circuit comprises a compensation circuit configured to generate an internal clock signal based on a clock received from the first clock input terminal signal compensating for a duty ratio deviation of the received clock signal, the internal clock signal swinging from a first voltage to a second voltage lower than the first voltage. Also, the present invention as now recited in claim 11 provides that a clock signal output circuit configured to delay the internal clock signal and output the delayed clock signal to the second liquid crystal drive circuit via the second clock signal line.

Someya is directed to a liquid crystal display which reduces sticking and ghosting of character and graphic images while a television signal and a character and graphics signal are displayed simultaneously. Someya shows a clock generator that generates various clock signals from the horizontal and vertical synchronizing signals. As the Examiner admitted, however, Someya does not disclose that the clock generator compensates a duty ratio deviation of the received clock signal.

Sasaki is directed to a liquid crystal display device capable of achieving a larger screen size or a higher resolution, without unnecessarily increasing the dimensions of the frame region and the manufacturing cost. Sasaki shows that a first latch circuit latches pixel data signal and control signals in response to the clock signal output from the first buffer amplifier, a delay cycle regulator that regulates a duty ratio with regard to the clock signal output from the buffer amplifier, and a second latch circuit latches the pixel data and the control signals output from the first latch circuit in response to the clock signal output from the duty cycle regulator. However, the first and second latch circuits in Sasaki are not liquid crystal drive circuit. They merely latch the pixel data signal. Furthermore, Sasaki does not explicitly or implicitly teach or suggest that the clock signal is delayed and the delayed clock signal is outputted to a second liquid crystal drive circuit.

Murata is directed to a liquid crystal display device capable of attaining accurate sampling of image data even where the operation speed is increased to achieve such an extra-high precision image display. Murata merely shows that a first clock signal and adjustment clock signals are generated, and image data are delayed by a specified time interval based on a corresponding adjustment clock signals to adjust the delay time of the first clock signal. Murata does not explicitly or implicitly teach or suggest that the clock signal itself is delayed Also, Murata does not explicitly or implicitly teach or suggest that the delayed clock signal is outputted to a second liquid crystal drive circuit.

Furthermore, there is no suggestion or motivation in Someya, Sasaki, or Murata to combine these features explicitly or implicitly, or in the knowledge generally available to one of ordinary skill in the art at the time the invention was made to embody all the features of the invention as recited in claim 11. Accordingly, claim 11 and dependent claims 12-15 are not obvious in view of all the prior art.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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July 1, 2006
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